AMENDMENTS TO THE SPECIFICATION

[0042] The H sync counter 82 is reset in synchronization with a vertical synchronizing signal from the vertical synchronizing signal generating unit 24 and counts output signals of the oscillator 42 to output horizontal synchronizing signals (H sync). The back-up V sync generating counter 86 counts horizontal synchronizing signals from the H sync counter 82 to generate back-up vertical synchronizing signals. However, the output of the generated vertical synchronizing signals is retained when a [[rest]] reset signal is inputted by the reset circuit 88. When the vertical synchronizing signal generating unit 24 fails to extract vertical synchronizing signals, a [[rest]] reset signal of the [[rest]] reset circuit [[99]] 88 is not outputted, and back-up vertical synchronizing signals of the back-up V sync generating counter 86 are outputted to the OR gate 80. The back-up vertical synchronizing signals are outputted also to an error counter 84, and times of the back-up vertical synchronizing signals having compensated vertical synchronizing signals are counted. The main CPU 30 can read counted values of the error counter 84.

[0043] As shown in FIGS. 7A and 7B, when vertical synchronizing signals have been extracted by the vertical synchronizing signal generating unit 24, [[rest]] reset signals prohibit the back-up V sync generating counter 86 from outputting back-up vertical synchronizing signals. However, when vertical synchronizing signals cannot be temporarily extracted from television signals due to radio wave troubles, etc., no [[rest]] reset signal is [[not]] outputted, and back-up vertical synchronizing signals generated by the back-up V sync generating counter 86 are outputted to the OR gate. Even when television signals are disturbed due to radio wave troubles, etc., stable vertical synchronizing signals are constantly outputted by the OR gate 80.